AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0009] The present invention, among other applications, is directed to solving the above-noted problems and addresses other problems, disadvantages, and limitations of the prior art. The present invention provides a superior technique for ensuring the coherency of instructions in a present day microprocessor pipeline in the presence of conditions induced by pending or concurrently executed store operations. In one embodiment, an apparatus in a pipeline microprocessor is provided, for ensuring coherency of instructions within stages of the pipeline microprocessor. The apparatus includes instruction cache management logic and synchronization logic. The instruction cache management logic receives an address corresponding to a next instruction to be fetched, and detects that a part of a memory page corresponding to the next instruction to be fetched cannot be freely accessed without checking for coherency of the instructions within the part of the memory page and, upon detection, provides the address. The synchronization logic receives the address from the instruction cache management logic. The synchronization logic directs data cache management logic to check for coherency of the instructions within the part of the memory page, and, if the instructions are not coherent within the part of the memory page, the synchronization logic directs the pipeline microprocessor to stall a fetch of the next instruction to be fetched until the stages of the pipeline microprocessor have executed all preceding instructions.

~~[0010] One aspect of the present invention contemplates an apparatus in a pipeline microprocessor, for ensuring coherency of instructions within stages of the pipeline microprocessor. The apparatus has data cache management logic and synchronization logic. The data cache management logic receives an address corresponding to a store instruction that is pending, and detects that a part of a memory page corresponding to the store instruction cannot be freely accessed without checking for coherency of the instructions within the part of the memory page, and, upon detection, provides the~~

~~address. The synchronization logic receives the address from the data cache management logic, and directs instruction cache management logic to check for coherency of the instructions within the part of the memory page, and, if the instructions are not coherent within the part of the memory page, the synchronization logic directs the pipeline microprocessor to flush preceding stages of the pipeline microprocessor.~~

[0011] Another aspect of the present invention comprehends a method in a pipeline microprocessor, for ensuring coherency of instructions within stages of the pipeline microprocessor. The method includes, within ~~a data cache~~an instruction cache, detecting that a part of a memory page corresponding to a ~~pending store~~ next instruction to be fetched ~~instruction~~ cannot be freely accessed without checking for coherency of the instructions within the part of the memory page; directing logic within ~~an instruction~~a data cache to check for coherency of the instructions within the part of the memory page ~~memory~~; and, if the instructions are not coherent, stalling a fetch of the next instruction from the instruction cache until the stages of the pipeline microprocessor have executed all preceding instructions~~flushing preceding stages of the pipeline microprocessor~~.